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ADVANCED DATASHEET - 03/02/99
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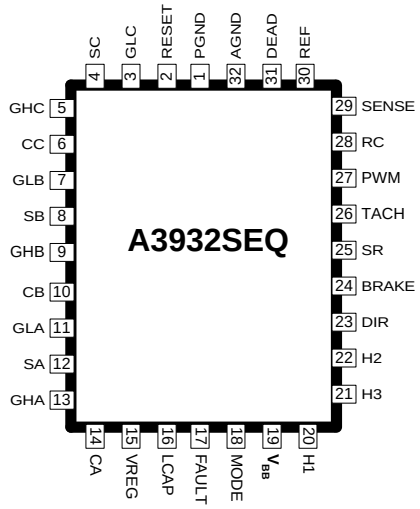
THREE PHASE POWER MOSFET CONTROLLER



ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Load Supply Voltage, V_{BB} ..... **50 V**
VREG (Transient) ..... **15 V**
Logic Input Voltage Range,
V_{IN} ..... **-0.3 V to V_{LCAP} + 0.3 V**
Sense Voltage, V_{SENSE} ..... **-5 to 1.5 V**
Pins SA/SB/SC, ... **-5 to 50 V**
Pins GHA/GHB/GHC ..... **-5 to V_{BB} + 17 V**
Pins CA/CB/CC ..... **SA/SB/SC+17 V**
Package Power Dissipation (T_A = +25°C)
$R_{\theta JA}$ ..... **52.4 °C/W**
$R_{\theta JC}$ ..... **22.7 °C/W**
P_D ..... **2.4 W**
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Junction Temperature, T_J ..... **+150°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

The A3932SEQ is a three-phase brushless DC motor controller. The A3932's high current gate drive capability allows driving of a wide range of power MOSFETs and can support motor supply voltages from 12 to 50V. The A3932 integrates a bootstrapped high side driver to minimize the external component count required to drive N-channel MOSFET drivers.

Internal fixed off time PWM current control circuitry can be used to regulate the maximum load current to a desired value. The peak load current limit is set by the user's selection of an input reference voltage and external sensing resistor. The fixed off time pulse duration is set by a user-selected external RC timing network. For added flexibility, the PWM input can be used to provide speed/torque control, allowing the internal current control circuit to set a maximum current limit.

The A3932 includes optional synchronous rectification. This feature will short out the current path through the power MOSFETs intrinsic body diodes during PWM off cycle current decay. This can minimize power dissipation in the MOSFETs, eliminate the need for external power clamp diodes, and potentially allow a more economical choice for the MOSFET drivers.

The A3932 provides commutation logic for Hall sensors configured for 120-degree spacing. The Hall input pins are pulled up to an internally generated 5V reference. Power MOSFET protection features includes gate-source voltage monitor, bootstrap capacitor charging current monitor, undervoltage monitor, motor lead short to supply or ground, and thermal shutdown.

FEATURES

- Drives Wide Range of N-channel MOSFETs
- Sources 1.25A for Gate Turn-On
- Sinks 2.5A for Gate Turn-Off
- Synchronous Rectification
- Power MOSFET Protection
- Adjustable Dead Time for Cross Conduction Protection
- Fast/Slow Current Decay Modes
- Internal PWM current Control
- PWM Torque Control Input
- Motor Lead Short to Supply and Ground Protection
- Internal 5V Regulator
- Direction Control
- Brake Input
- Fault Diagnostic Output
- Tachometer Output
- Thermal Shutdown
- Undervoltage Protection
- 32L PLCC Package

Always order by complete part number: **A3932SEQ**

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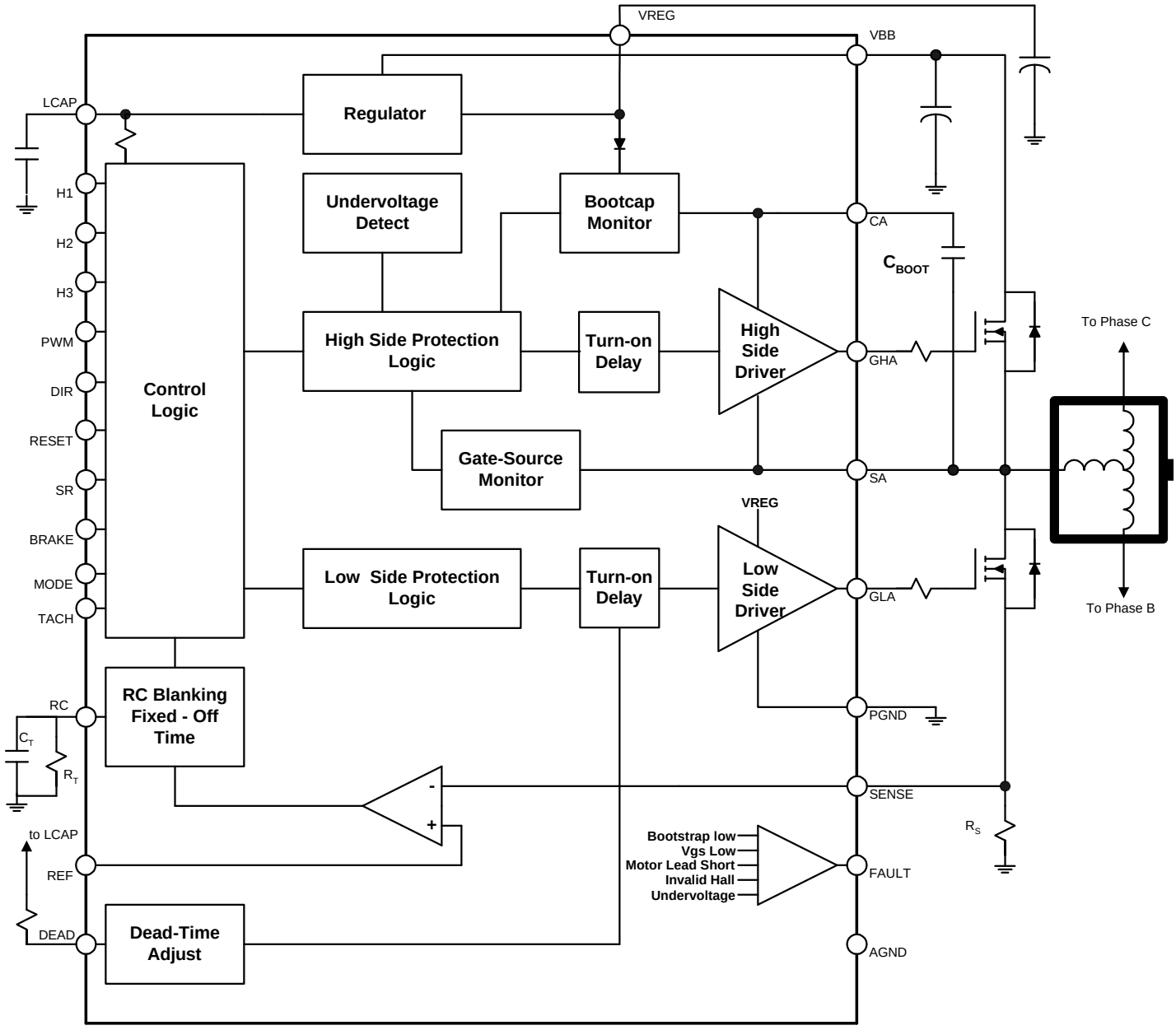
Functional Block Diagram (1 of 3 outputs shown)



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ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 50 V, C_{BOOT}= .1µf, C_{LOAD}=1000pf (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Quiescent current	I_{VBB}	RESET Low		6.5	8.5	mA
	I_{VBB}	RESET High			6.5	mA
LCAP Regulator	V_{LCAP}		4.75	5	5.250	V
Motor Supply Voltage Range			18	–	50	V
		VREG shorted to V_{BB}	10.8	–	13.2	V
VREG Output Voltage	V_{REG}		12.4	13	13.6	V
VREG Line Regulation	V_{REGLIN}	V_{BB} 18 to 50V	–	40	–	mV
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		2.0	–	–	V
	$V_{IN(0)}$		–	–	.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.0 V	–	<1.0	10	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V	-70	–	-130	µA
Gate Drive						
Low side drive, output high	V_{HGL}		12.3	13	13.7	V
High side drive, output high	V_{HGH}		10.5	11.6	12.8	V
Pull Up Switch Resistance	$R_{DS(ON)}$	-1A transient	6	9	12	Ω
Pull Down Switch Resistance	$R_{DS(ON)}$	2.5A transient	2	3	4	Ω
Low side switching, rise time	tr_{GL}	10% to 90%	–	25	–	ns
Low side switching, fall time	tf_{GL}		–	10	–	ns
High side switching, rise time	tr_{GH}		–	40	–	ns
High side switching, fall time	tf_{GH}		–	10	–	ns
Dead time maximum	t_{DEAD}	I_{DEAD} = 9µA	–	5500	–	ns
Dead time minimum	t_{DEAD}	I_{DEAD} = 780µA	–	100	–	ns

NOTES:
1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device pin.

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Bootstrap Capacitor						
Bootstrap Capacitor Voltage	V_{CAP}		10.4	11.6	12.8	V
Bootstrap Charge Threshold	$I_{BOOTCHG}$		9	13	18	mA
Bootstrap Capacitor R_{OUT}	R_{CAP}			5	8	Ω
Charge Current	I_{CX}		100			mA
CAP Leakage Current	I_{CAP}	High Side switched ON		15	25	µA
Current Limit Circuitry						
Offset Voltage	V_{IO}		-5	0	5	mV
Input Bias Current	I_B		-5		0	µA
Comparator Common Mode Range	V_{CMR}		0		1.5	V
RC Charge Current	I_{RC}		.9	1	1.1	µA
RC Voltage Threshold	V_{RCL}		1.0	1.1	1.2	V
	V_{RCH}		2.7	3.0	3.3	V
Protection Circuitry						
Gate Source Monitor	$UVLO_{GS}$	V_{CAP}-V_{GHX}, High Side Switched ON	2.7	3.3	3.9	V
Short to Ground, Drain-Source Monitor	$UVLO_{DS}$	V_{BB}- V_{SX}, High Side ON	1.6	2.0	2.4	V
Undervoltage Threshold	UVLO	V_{REG} low to High	9.4	9.9	10.4	V
	UVLO	V_{REG} High to Low	8.8	9.3	9.8	V
Fault Output	V_{FAULT}	I_{OL} = 1mA			.5	V
Tach Output	V_{TACH}	I_{OL}= 500 µA			.5	V
Thermal Shutdown Temp.	T_J		–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J		–	10	–	°C

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Pin Descriptions

RESET. A logic input that enables the device, internally pulled up to LCAP. Logic HIGH will disable the device and turn off MOSFETs, coasting the motor. Logic LOW will enable gate drive to follow commutation logic. This input will override BRAKE.

GLC/GLB/GLA. Low side gate drive outputs for external MOSFET drivers. External series gate resistors can be used to control slew rate seen at the power driver gate, thereby controlling the di/dt and dv/dt of S outputs. The outputs will source 1.25A for turn-on and sink 2.5A for gate discharge.

SC/SB/SA. Directly connected to the motor terminals, these pins sense the voltages switched across the load. The pin is also connected to the negative side of the bootstrap capacitor and negative supply connection for the floating high side drive.

GHC/GHB/GHA. High side gate drive outputs for n-channel MOSFET drivers. External series gate resistors can be used to control slew rate seen at the power driver gate, thereby controlling the di/dt and dv/dt of S outputs. The outputs will source 1.25A for turn-on and sink 2.5A for gate discharge.

CC/CB/CA. High side connection for bootstrap capacitor, positive supply for high side gate drive. The bootstrap capacitor is charged to approximately VREG when the output Sx terminal is low. When the output swings high, the voltage on this pin rises with the output to provide the boosted gate voltage needed for N-channel power MOSFETs.

MODE. Logic input to set current decay method. Slow decay mode (logic HIGH) switches off the high side FET in response to PWM Off command. Fast decay mode (logic LOW) switches off the source and sink MOSFET's. Mode pin is internally pulled up to LCAP.

H1/H2/H3. Hall sensor inputs, internally pulled up to LCAP. Configured for 120-degree electrical spacing.

DIR. Logic input to reverse rotation, see commutation logic table. Internally pulled up to LCAP.

FAULT. Open drain output to indicate fault condition. Will go active high for any of the following fault conditions:

1) Invalid HALL input code.
2) High side gate-source undervoltage.
3) Bootstrap capacitor not sufficiently charged.
4) Undervoltage condition detected at VREG.
5) Thermal Shutdown.
6) Motor lead (SA/SB/SC) connected to ground.

Any fault will force a COAST condition, which turns all power MOSFETs off. The fault state for gate-source and bootstrap monitors is cleared at each commutation. If the motor has stalled, the fault must be cleared by toggling the RESET pin or repeating a power up sequence.

BRAKE. Logic input for braking function. Logic LOW will turn on sink side MOSFETs, turn off the source side MOSFETs. This will effectively short the BEMF in the windings and brake the motor. Internally pulled up to logic LCAP.

SR. Synchronous rectification input. Logic LOW disables the feature forcing current decay through flyback diodes. Logic HIGH will result in the opposite pair of drivers to switch in response to a PWM "off" command. Internally pulled up to LCAP.

TACH. Digital output to indicate speed of rotation. A 3µs pulse appears at every Hall transition.

PWM. Speed control input. Logic HIGH will turn on MOSFETs selected by Hall input logic. Logic LOW turns off the selected MOSFETs. The PWM input held high to utilize internal current control circuitry. Internally pulled up to logic LCAP.

RC. Analog input. Connection for R_T and C_T to set the fixed off time. The C_T will also set the BLANK time. (see applications information). It is recommended that the fixed off time should not be less than 10µs. The resistor should be in the range 10k to 500k.

SENSE. Analog input to the current limit comparator. Voltage representing load current appears on this pin. Voltage transients seen at this pin when the drivers turn on are ignored for time T_{blank}.

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PIN DESCRIPTIONS (continued)

VREG. Regulated 13 V output supply for low side gate drive and bootstrap capacitor charge circuit. It is good practice to connect a decoupling capacitor from this pin to AGND, as close to the device pins as possible. Pin should be shorted to VBB for 12V applications.

V_{BB}. Motor power supply connection for A3932 and power MOSFETs. Pin should be shorted to VREG for 12V applications.

REF. Analog input to current limit comparator. Voltage applied here sets the peak load current according to the equation:

$$I_{TRIP} = V_{REF}/R_{SENSE}$$

LCAP. 5V reference to power internal logic, connection for decoupling cap. This pin requires 1nF external capacitor for decoupling and should not be used to power any external circuitry.

DEAD. Analog input. A resistor between DEAD and LCAP is selected to adjust turn-off to turn-on time. This delay is needed to prevent shoot-thru in the external power FET's. The resistor allowable range is 5.6k to 470k, which converts to deadtime of 100ns to 5500ns.

$$T_{DEAD} \cong 11e\text{-}12 * R_{DEAD}$$

AGND. Analog reference.

PGND. Return for low side gate drive. This should be connected to PCB power ground.

Commutation Truth Table

H1	H2	H3	DIR	GLA	GLB	GLC	GHA	GHB	GHC	SA	SB	SC
1	0	1	1	0	0	1	1	0	0	HI	Z	LO
1	0	0	1	0	0	1	0	1	0	Z	HI	LO
1	1	0	1	1	0	0	0	1	0	LO	HI	Z
0	1	0	1	1	0	0	0	0	1	LO	Z	HI
0	1	1	1	0	1	0	0	0	1	Z	LO	HI
0	0	1	1	0	1	0	1	0	0	HI	LO	Z
1	0	1	0	1	0	0	0	0	1	LO	Z	HI
1	0	0	0	0	1	0	0	0	1	Z	LO	HI
1	1	0	0	0	1	0	1	0	0	HI	LO	Z
0	1	0	0	0	0	1	1	0	0	HI	Z	LO
0	1	1	0	0	0	1	0	1	0	Z	HI	LO
0	0	1	0	1	0	0	0	1	0	LO	HI	Z

INPUT LOGIC

MODE	PWM	S/R	RESET	Quadrant	Mode of Operation
0	0	0	0	Fast decay	PWM chop– current decay, all drivers off
0	1	0	0	Fast Decay	Peak Current limit – selected drivers ON
1	0	0	0	Slow decay	PWM chop – current decay, selected Low side ON
1	1	0	0	Slow Decay	Peak Current limit mode – selected drivers ON
0	0	1	0	Fast decay	PWM chop – current decay with opposite of selected drivers ON
0	1	1	0	Fast Decay	Peak Current limit – selected drivers ON
1	0	1	0	Slow decay	PWM chop – current decay with both Low side drivers ON
1	1	1	0	Slow Decay	Peak Current limit – selected drivers ON
X	X	X	1	X	All gate drive outputs to 0V – Clear fault logic

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APPLICATION INFORMATION

Synchronous Rectification. To reduce power consumption in the external MOSFETs, the 3932 control logic will turn on the appropriate driver during the load current recirculation, PWM "off" cycle. The intrinsic body diode of the power MOSFET will only conduct during the dead time required at each PWM transition.

Decoupling. The internal reference VREG supplies current for the gate drive circuit. As the gates are driven high they will require current from an external decoupling capacitor to support the transients. This capacitor should be placed as close as possible to the VREG pin. The value of the capacitor should be at least 20 times larger than the bootstrap capacitor. Additionally, a 1nF ceramic monolithic capacitor should be connected between LCAP and AGND as close to the device pins as possible.

Protection Circuitry. The A3932 will protect the external MOSFETs by turning off all MOSFETs if any of the following fault conditions are detected.

1) **Gate Source Monitor (high side only).** The voltage on GHx pins must stay within 3.3V of the bootstrap capacitor voltage during an ON cycle. If this voltage droops below this threshold the high side turns off, and the low side gate will turn on in an attempt to recharge the bootstrap capacitor. When the bootstrap capacitor has been properly charged, the high side is turned back on. The circuit will allow three faults of this type within one commutation cycle before signaling a fault and coast the motor.

2) **Bootstrap Monitor**. The bootstrap capacitor is charged whenever a sink side FET is on, Sx output goes low, and load current recirculates. This happens constantly during normal operation. A 170µs timer is started at the beginning of this cycle and the capacitor is charged with typically 100 mA. If the charge current remains higher than 13mA or the Sx node remains higher than 2V for longer than the 170µs a fault will be signaled and the motor will coast.

3) **Undervoltage**. VREG supplies the low side gate driver and the bootstrap charge current. It is critical to ensure that the voltages are at a proper level before enabling any of the outputs. The undervoltage circuit is active during power up and will force a motor coast condition until VREG is greater than approximately 10V.

4) **Hall Invalid**. Illegal codes for the hall inputs (000/111) will force a fault and coast the motor.

5) **Thermal Shutdown**. Junction temperature greater than 165°C will signal a fault and coast the motor.

6) **Motor Lead**. The 3932 will signal a fault if the motor lead is shorted to ground or supply. The status is checked after any high side has turned on.

Faults are cleared at the beginning of each commutation. If a stalled motor results from a fault, the fault can only be cleared by toggling the RESET pin or by a power up sequence.

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Current Regulation. Load current is regulated by an internal fixed off time PWM control circuit. When the outputs of the MOSFETs are turned on, current increases in the motor winding until it reaches a value given by:

$$I_{TRIP} = V_{REF} / R_{SENSE}$$

At the trip point, the sense comparator resets the source enable latch, turning off the source driver. At this point, load inductance causes the current to recirculate for the fixed off time period. The current path during recirculation is determined by the configuration of the MODE and SR input pins. The fixed off time is determined by an external resistor (R_T) and capacitor (C_T) connected in parallel from the RC terminal to AGND. The fixed off time is approximated by:

$$t_{OFF} = R_T * C_T$$

T_{OFF} should be in the range 10µs to 50µs. Larger values for T_{OFF} could result in audible noise problems.

Torque control can be implemented by varying the REF input voltage as long as the PWM input stays high. If direct control of the torque/current is desired by PWM input, a voltage can be applied to the REF pin to set an absolute maximum current limit.

PWM Blank. The capacitor (C_T) also serves as the means to set the BLANK time duration. At the end of a PWM off cycle, a high side gate selected by the commutation logic will turn on. At this time, large current transients can occur during the reverse recovery time (trr) of the intrinsic body diodes of the power MOSFETs. To prevent false tripping of the sense comparator, the blank function will disable the comparator for a time defined by:

$$T_{BLANK} = (1.9 * C_T)/(1mA\text{-}2/ R_T)$$

The user must ensure that the C_T is large enough to cover the current spike duration.

Braking. The 3932 will dynamically brake by forcing all sink side MOSFETs on, and all source side MOSFETs off. This will effectively short out the BEMF and brake the motor. During braking the load current can be approximated by:

$$I_{BRAKEPEAK} = V_{BEMF}/R_{LOAD}$$

As the current does not flow through the sense resistor during a dynamic brake, care should be taken to ensure that the power MOSFETs maximum ratings are not exceeded.

The RESET pin overrides the BRAKE input. RESET will always drive all gate outputs Low.